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(71) Applicant: SHINKO ELECTRIC INDUSTRIES CO. LTD.
Nagano-shi, Nagano 380-0921 (JP)

(72) Inventors:
- Rokugawa, Akio, c/o Shinko Elec. Ind. Co., Ltd.
Nagano-shi, Nagano 380-0921 (JP)
- Iijima, Takahiro, c/o Shinko Elec. Ind. Co., Ltd.
Nagano-shi, Nagano 380-0921 (JP)
- Nomura, Tomohiro,
c/o Shinko Elec. Ind. Co., Ltd.
Nagano-shi, Nagano 380-0921 (JP)
- Koyama, Toshinori,
c/o Shinko Elec. Ind. Co., Ltd.
Nagano-shi, Nagano 380-0921 (JP)
- Katagiri, Noritaka, Shinko Elec. Ind. Co., Ltd.
Nagano-shi, Nagano 380-0921 (JP)

(74) Representative: Rackham, Stephen Neil
GILL JENNINGS & EVERY,
Broadgate House,
7 Eldon Street
London EC2M 7LH (GB)

(54) Multilayer circuit board

(57) A process for making a multilayer wiring board includes the following steps of: laminating an electrically insulating resin substrate (34), having first and second surfaces and a metal layer (36) formed on the first surface, onto a base material (32) on which a predetermined wiring pattern (30) is formed, so that the second surface of the resin substrate (34) is adhered to the base material (32): removing a predetermined amount (38) of the metal layer (36) to form an opening at a position where a connection with the wiring pattern (30) is to be provided; irradiating a laser beam toward the resin layer (34) through the resin removed region (38) to form a blind via hole (40) having a diameter smaller than that of the opening (38), so that the wiring pattern (30) is exposed at a bottom of the blind via hole (40); electroless plating form an electroless plated film on the exposed wiring pattern (30), a side wall of the blind via hole (40), a step layer (36) at a periphery of the opening (40); electro plating to form an electro plated film on the electroless plated film; and after the electro plating, etching the metal layer to form a predetermined wiring pattern (36a).

Fig.1(d)

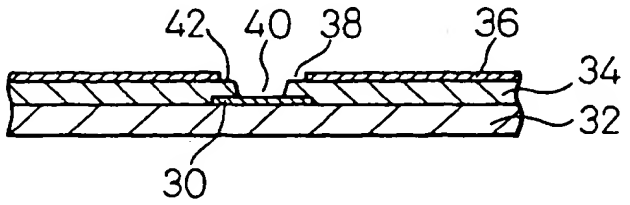

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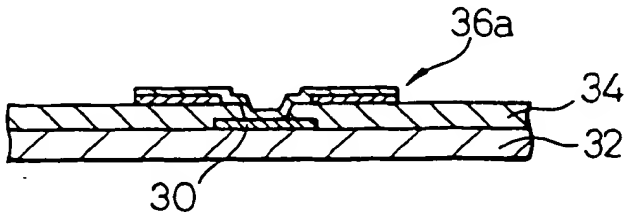
Fig.1(f)



Description

[0001] The present invention relates to a process for producing a multilayer circuit board and, more particularly, to a process for producing a multilayer circuit board having a blind via hole which is filled with plated film.

[0002] Various processes for making a multilayer circuit board are conventionally known.

[0003] Figs. 5(a) to 5(c) shows one of the known processes for producing a multilayer circuit board.

[0004] First, on a resin base 12 on which a wiring pattern is formed, a metal foil, such as a copper foil or the like, with an adhesive resin layer, such as a pre-preg or polyimide resin layer, is laminated and heat-pressed so that the metal foil 16 is adhered onto the resin base 12, as shown in Figs. 5(a) and 5(b).

[0005] Then, using a metal plate as a masking, a blind via hole 18 is formed by a carbon dioxide gas laser through the metal foil 16 and the resin layer 14 so that a part of the wiring pattern 10 is exposed, as shown in Fig. 5(c).

[0006] Then, an electroless-copper plating or electro-copper plating is applied to the blind via hole 18 to form a plated film 20 to attain an electrical connection between the wiring pattern 10 and the metal foil 16, as shown in Fig. 5(d).

[0007] Then, the metal foil 16 is etched to form a predetermined wiring pattern (not shown).

[0008] The above-mentioned processes are repeated for several times and, thereby, a multilayer circuit board can be obtained.

[0009] Figs. 6(a) and 6(b) show another known process for producing a multilayer circuit board.

[0010] In this process, on the resin base 12 on which a wiring pattern is formed, a photosensitive resin layer 22 is formed, as shown in Fig. 6(a).

[0011] Then, the photosensitive resin layer 22 is etched by a photolithographic method to form a blind via hole 24 which reaches to a circuit pattern, a plated film 26 is formed on the blind via hole 24 and the resin layer 22 by a sputtering process and an electro-plating process, as shown in Fig. 6(c), and the plated film formed on the resin layer 22 is etched to form a desired circuit pattern.

[0012] As mentioned above, there are various known processes for producing a multilayer circuit board. In the known method shown in Figs. 6(a) and 6(b), an electro-plated film is formed on the resin layer 22 through the sputtered film but the adhesivity between the resin layer 22 and the sputtered film is not strong. Thus, a problem of peeling-off will occur.

[0013] In the process shown in Figs. 5(a) to 5(d), since the metal foil 16 is beforehand adhered to the resin layer 14 with a predet rmined strength, a multilayer circuit board having a good adhesivity with the resin material can thus be provided.

[0014] However, the following problems will arise even in the process shown in Figs. 5(a) to 5(d).

[0015] R cently, there is a great demand that the circuit pattern should be very dense and sophisticated. Therefore, the width of line becomes very narrow and thus it is required that the diameter of the above-mentioned blind via 18 for connecting upper and lower circuit patterns therebetween must be made very small.

[0016] In addition, the blind via hole 18 is generally formed by a carbon dioxide laser as mentioned above. In this case, however, such a carbon dioxide laser is limited to form a hole, the diameter thereof being 80 μm or more. Consequently, it is impossible to form such a via hole, the diameter thereof being less than 80 μm, using a carbon dioxide laser.

[0017] In a process during which the diameter of the blind via hole 18 becomes very small, if the plated film 20 is formed by an electro-plating process, as shown in Fig. 7, the electric current may be concentrated at the angle portion A of the metal foil 16, i.e., an inlet edge of the blind via hole 18. As a result of the electric current being concentrated at the angle portion A, the inlet edge of the blind via hole 18 may become "necked", the diameter of the inlet portion being narrow, and the plating liquid may enter therein and affectedly influence the plated film. On the contrary, the diameter deep inside the blind via hole 18 becomes relatively large and the thickness of the plated layer becomes thin. Thus, an electrical disconnection may occur in the blind via hole.

[0018] An object of the present invention is to provide a process for producing a multilayer circuit board in which a blind via hole of a small diameter can be made and high density wiring can be provided.

[0019] Another object of the present invention is to provide a process for producing a multilayer circuit board in which the above-mentioned drawbacks can be overcome.

[0020] According to the present invention, there is provided a process for producing a multilayer wiring board comprising the following steps of: laminating an electrically insulating resin substrate, having first and second surfaces and a metal layer formed on the first surface, onto a base material on which a predetermined wiring pattern is formed, so that the second surface of the resin substrate is adhered to the base material; removing a predetermined range of the metal layer to form an opening at a position where a connection with the wiring pattern is to be provided; irradiating a laser beam toward the resin layer through the resin removed region to form a blind via hole having a diameter smaller than that of the opening, so that the wiring pattern is exposed at a bottom of the blind via hole; electroless plating to form an electroless plated film on the exposed wiring pattern, a side wall of the blind via hole, a step portion of the exposed resin layer, and at least a metal layer at a periphery of the opening; electro plating to form an electro plated film on the electroless plated film; and after the electro plating, etching the metal layer to form a predetermined wiring pattern.

[0021] The laser beam irradiating step comprises a

step of irradiating a laser beam having a wavelength in the ultraviolet range

[0022] According to another aspect of the present invention, there is provided a process for producing a multilayer wiring board comprising the following steps of: forming a resin layer onto an electrically insulating base material on which a predetermined wiring pattern is formed, adhering a metal layer onto the resin layer; removing a predetermined amount of the metal layer to form an opening at a position where a connection with the wiring pattern is to be attained; irradiating a laser beam toward the resin layer through the resin removed region to form a blind via hole having a diameter smaller than that of the opening so that the wiring pattern is exposed at a bottom of the blind via hole; electroless plating to form an electroless plated film on the exposed wiring pattern, a side wall of the blind via hole, a step portion of the exposed resin layer, and at least a metal layer at a periphery of the opening; electro plating to form an electro plated film on the electroless plated film; and after the electro plating, etching the metal layer to form a predetermined wiring pattern.

[0023] According to still another aspect of the present invention, there is provided a process for producing a multilayer wiring board comprising the following steps of: laminating an electrically insulating resin substrate onto a base material on which a predetermined wiring pattern is formed, so that a surface of the resin substrate covers the wiring pattern; irradiating a laser beam toward the resin layer to form a blind via hole, so that the wiring pattern is exposed at a bottom of the blind via hole; electroless plating to form an electroless plated film on the exposed wiring pattern and a side wall of the blind via hole; forming a resist on the electroless plated film except for the region of the via hole and a peripheral area thereof; electro plating to form an electro plated film on the electroless plated film except for the resist; and removing the resist and subsequently the electroless plated film under the resist.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024]

Figs. 1(a) to 1(f) are cross-sectional views illustrating an embodiment of a process for producing a multilayer wiring board according to the present invention.

Figs. 2(a) and 2(b) are cross-sectional views illustrating another embodiment according to the present invention;

Fig. 3 is a cross-sectional view for explaining a blind via hole filled with a plated film;

Figs. 4(a) to 4(i) are cross-sectional views illustrating still another embodiment according to the present invention;

Figs 5(a) to 5(d) are cross-sectional views illustrating a process for producing a multilayer wiring board known in the prior art;

Figs. 6(a) and 6(b) are cross-sectional views illustrating another known process for producing a multilayer wiring board; and

Fig. 7 is a cross-sectional view for explaining an example in which the blind via hole is filled with a plated film in a "necked" manner.

[0025] In the drawings, Figs. 1(a) to 1(f) show a first embodiment of this invention.

[0026] A circuit pattern 30 is formed on the base substrate 32 (a printed circuit board, a ceramic circuit board, or the like). A resin substrate with metal foil, which comprises an adhesive resin layer 34, such as a pre-preg, a polyimide resin layer or the like, formed on one surface of a metal foil 36, such as a copper foil, is laminated on the circuit pattern 30, as shown in Fig. 1(a).

[0027] The resin layer 34 is then pressed and heated to harden the same so that the substrate 32 is adhered to the metal foil 36 through the resin layer 34.

[0028] Then, the metal foil 36 at the portion of the lands corresponding to the connecting portion of the blind via connecting portion is removed by an etching process or a laser process to form an opening 38 so that a part of resin layer 34 is exposed, as shown in Fig. 1(c).

[0029] It is preferable that the diameter X of the opening 38 is smaller than the diameter C of the land of the wiring pattern 30. As mentioned hereafter, the position of the opening 38 is made as connecting portion between the upper and lower wiring patterns. Since the diameter of this connecting portion is smaller than the diameter C of the land, the wiring density thereof is not affected and high density wiring can thus be attained.

[0030] A resin substrate with metal foil, in which an opening is beforehand provided at a position of the metal foil corresponding to the lands of the wiring pattern, can also be laminated with each other.

[0031] A blind via hole 40 is formed at a position of the resin layer 34 at which the resin layer 34 is exposed and the exposed portion becomes the bottom of the blind via hole 30, as shown in Fig. 1(d). The diameter of the blind via hole 40 is smaller than that of the opening 38.

[0032] The blind via hole 40 can be formed by a laser process. As mentioned hereinbefore, a carbon dioxide laser is not suitable since it is difficult to bore a hole having a diameter of less than 80 μm by a carbon dioxide laser. Although a mask, i.e., a metal mask, can be used to form such a hole having a small diameter, the productivity of such method is relatively now.

[0033] Therefore, it is suitable to use a YAG laser or IRF laser, without using any masking, to bore a hole which has a diameter of more or less 30 μm, in which the wavelength is in the ultraviolet range so as to reduce the diameter thereof.

[0034] Otherwise, it is also suitable to bore a hole having a small diameter by an excimer laser, the wavelength thereof being in the ultraviolet range.

[0035] The carbon chain of the resin layer 34 can be cut so that the resin layer 34 is resolved and removed by irradiating a laser beam having wavelength in the ultraviolet range.

[0036] The laser beam can be reduced to a small beam diameter and the diameter of the opening 38 can be made larger within the range of the land of the wiring pattern. The alignment, when the laser beam is irradiated. can easily be performed. Since the diameter of the blind via hole 40 is smaller than the diameter of the opening 38. a step portion 42 of the resin layer 34 can thus remain around the periphery of the opening of the blind via hole 40.

[0037] After any processing wastes due to the laser beam processing are removed, an electroless plated layer such as a copper layer, is formed on the surface of the wiring pattern 30, the side wall of the blind via hole 40, the exposed step portion 42 of the resin layer 34 and at least the surface of the metal foil 36, such as copper foil around the opening 38. Then, an electro plated layer 44 is formed on this electroless plated layer, as shown in Fig. 1(e)

[0038] Then, as shown in Fig. 1(f), a predetermined wiring pattern 36a is formed by etching the metal foil 36.

[0039] The above-mentioned processes are repeated and. thus. on the wiring pattern 36a, a multilayer wiring pattern is formed.

[0040] As mentioned above, according to the embodiment of this invention, the diameter of the opening 38 is larger than the diameter of the blind via hole 40 and, therefore, the step portion 42 remains on the resin layer 34. The edge of the opening 38 of the metal foil 36 is removed from the opening edge of the via hole 40 and, therefore, when an electroplated film 44 is formed, even if the electric current is concentrated to the corner portion of the metal foil 36 at the edge of the opening 38 and, thus, the thickness of the plated film at the corner portion becomes larger, the recess comprising the opening 38 and the blind via hole 40 does not become a "neck". different from the prior art shown in Fig. 3. Since the inlet portion is wide open, the plating liquid does not remain in the recess and the flow of the plating liquid can be maintained. Therefore. the plated film can be formed smoothly even at the bottom portion of the via hole 40

[0041] Figs. 2(a) and 2(b) show a second embodiment of this invention. In this embodiment, as shown in Fig. 2(a), a base material, such as a printed circuit board on which a circuit pattern 30 is formed, is coated with a resin such as a polyimide resin, and is heated to form a resin layer 34 This resin layer 34 can also be formed on the base material by laminating a resin film.

[0042] Then, as shown in Fig. 2(b), a metal foil 36 is adhered onto the resin layer 34 by means of an adhesive.

[0043] The subsequent processes are the same as the steps as described and shown in Figs 1(c) to 1(f) and therefore a detailed explanation thereof is omitted. In this second embodiment, the same effects and advantages as the first embodiment can be obtained.

[0044] According to the present invention, after the blind via hole 40 is formed as shown in Fig. 1(d), an electroless copper plating is conducted and then an electro copper plated film 44 is formed as shown in Fig. 1(e). At this time, by the results of an experiment, it was confirmed that the blind via hole 40 could be substantially covered by the electro-copper plated film 44, as shown in Fig. 3. That is to say, the density of electric current when conducting the electro copper plating could be reduced to less than an ordinary density of electric current (2 to 3 ASD).

[0045] Usually, the inside area of the blind via hole 40 restricts a flow of the plating material more than a flat surface, such as a surface of the conductive layer 36 formed on the resin layer 34. However, it was confirmed that since the density of electric current could be reduced by 0.1 to 2 ADS, preferably by around 1 ADS, the difference in the plating deposition speed between the flat surface and the inside of the blind via hole 40 was uniform, or otherwise the plating deposition speed at the blind via hole 40 was higher than that on the flat surface.

[0046] If the plating deposition speed at the blind via hole 40 becomes higher, the plating film can heap up not only at the bottom surface of the blind via hole 40, but also at the side surface thereof. Therefore, the thickness t_2 of the plated film from the bottom becomes larger than the thickness t_1 of the plated film at the flat surface and therefore it is possible to completely cover the blind via hole 40.

[0047] If the plating deposition time was increased to form a thick plated film, the blind via hole 40 could finally be covered completely with the plated film. However, as the result of a reduction in the density of electric current as mentioned above, when the diameter of the opening of the blind via hole 40 was 50 μm and the depth thereof was 40 μm, in which the thickness of the metal foil 36 (the thickness thereof being 5 μm) and the thickness t_1 of the plated film (the sum of the thickness of the electroless plated film and the thickness of the electro plated film) was 20 μm, the inside of the blind via hole 40 could substantially be covered by the plated film.

[0048] In order to fill the inside of the blind via hole 40 with the plated film, the most important factor is to reduce the density of electric current in the process of electro plating.

[0049] The other factors will be considered as follows.

[0050] First of all, the following conditions of the electroless plating are the most preferable.

the deposition speed: 0.2 to 3 μm/hr, and
the thickness of the plated film: 0.5 to 3.0 μm.

[0051] Also, it is preferable that the blind via hole 40 is tapered in such a manner that the inlet portion thereof is enlarged, since the plating liquid can circulate easily and deposition efficiency is improved.

[0052] In addition, assuming that the diameter of the opening of the blind via hole 40 was r, the depth thereof was h, the aspect ratio h/r was preferably 0.5 to 1.5.

[0053] Under the above-mentioned conditions:

$$t_2 > t_1,$$

and

$$t_2 > h/2,$$

a plated film having a thickness t_2 of the plated film can be obtained, in which t_2 satisfies the above conditions.

[0054] The diameter r of the opening of the blind via hole 40 is preferably 20 to 100 μm and the depth h thereof is preferably 20 to 100 μm. Therefore, the aspect ratio h/r is preferably 0.5 to 1.5 as mentioned above.

[0055] In order to fill the inside of the blind via hole 40 with the plated film, it is not always necessary to remove the metal foil 36, existing around the blind via hole 40, from around the opening, as illustrated. Even if there is no metal foil 36, it will be possible to fill the blind via hole 40 with the plated film.

[0056] Figs. 4(a) to 4(i) show a process for producing a multilayer wiring board of still another embodiment according to the present invention.

[0057] Figs. 4(a) and 4(b) corresponds to Fig. 1(a) and 1(b), respectively, and therefore a detailed explanation is omitted. In Fig. 4(c), the copper foil 36 is completely removed from the upper surface of the adhesive resin layer 34. Then, a blind via hole 40 is formed by a laser process at a position of the resin layer 34 by which the resin layer 34 is exposed and the exposed portion becomes a bottom of the blind via hole 40, as shown in Fig. 4(d).

[0058] Then, an electroless plated layer 46, such as a copper layer, is formed on the surface of the wiring pattern 30, the side wall of the blind via hole 40, the surface of the resin layer 34 around the blind via hole 40, as shown in Fig. 4(d). Then, a resist 48 is formed on the resin layer 34 except for the area of the blind via hole 40 and the peripheral region thereof, as shown in Fig. 4 (f). Then, an electro plated layer 44 is formed on this electroless plated layer, except for the area covered by the resist 48, as shown in Fig. 4(g). Then, the resist 48 is removed by a known process, as shown in Fig. 4(h) and also the electroless plated layer 46 is removed by etching, as shown in Fig. 4(i).

Claims

1. A process for producing a multilayer wiring board comprising the following steps of:

   laminating an electrically insulating resin substrate, having first and second surfaces and a metal layer formed on the first surface, onto a base material on which a predetermined wiring pattern is formed, so that the second surface of the resin substrate is adhered to said base material;

   removing a predetermined amount of said metal layer to form an opening at a position where a connection with said wiring pattern is to be attained;

   irradiating a laser beam toward said resin layer through said resin removed region to form a blind via hole having a diameter smaller than that of said opening, so that said wiring pattern is exposed at a bottom of said blind via hole;

   electroless plating to form an electroless plated film on said exposed wiring pattern, a side wall of said blind via hole, a step portion of said exposed resin layer, and at least a metal layer at a periphery of said opening;

   electro plating to form an electro plated film on said electroless plated film; and

   after said electro plating, etching said metal layer to form a predetermined wiring pattern.

2. A process as set forth in claim 1, wherein a diameter of said opening of the metal layer is larger than a diameter of said blind via hole.

3. A process as set forth in claim 1, wherein said laser beam irradiating step comprises a step of irradiating a laser beam having a wavelength in the ultraviolet range.

4. A process for producing a multilayer wiring board comprising the following steps of:

   forming a resin layer onto an electrically insulating base material on which a predetermined wiring pattern is formed;

   adhering a metal layer onto said resin layer;

   removing a predetermined amount of said metal layer to form an opening at a position where a connection with said wiring pattern is to be attained;

   irradiating a laser beam toward said resin layer through said resin removed region to form a blind via hole having a diameter smaller than that of said opening, so that said wiring pattern is exposed at a bottom of said blind via hole;

   electroless plating to form an electroless plated film on said exposed wiring pattern, a side wall of said blind via hole, a step portion of said exposed resin layer, and at least a metal layer at the periphery of said opening;

   electro plating to form an electro plated film on said electroless plated film; and

after said electro plating, etching said metal layer to form a predetermined wiring pattern.

5. A process as set forth in claim 4, wherein a diameter of said opening of the metal layer is larger than a diameter of said blind via hole.

6. A process as set forth in claim 4, wherein said laser beam irradiating step comprises a step of irradiating a laser beam having a wavelength in the ultraviolet range.

7. A process for producing a multilayer wiring board comprising the following steps of:

laminating an electrically insulating resin substrate onto a base material on which a predetermined wiring pattern is formed, so that a surface of the resin substrate covers said wiring pattern,
irradiating a laser beam toward said resin layer to form a blind via hole, so that said wiring pattern is exposed at a bottom of said blind via hole;
electroless plating to form an electroless plated film on said exposed wiring pattern and a side wall of said blind via hole;
forming a resist on electroless plated film except for the region of said via hole and the periphery thereof;
electro plating to form an electro plated film on said electroless plated film except for said resist; and
removing said resist and subsequently said electroless plated film under said resist.

8. A process as set forth in claim 7, wherein said laser beam irradiating step comprises a step of irradiating a laser beam having a wavelength in the ultraviolet range.

9. A process for producing a multilayer wiring board comprising the following steps of:

laminating an electrically insulating resin substrate, having first and second surfaces and a metal layer is formed on the first surface, onto a base material on which a predetermined wiring pattern is formed, so that the second surface of the resin substrate is adhered to said base material;
removing said metal layer;
irradiating a laser beam toward said resin layer to form a blind via hole, so that said wiring pattern is exposed at a bottom of said blind via hole;
electroless plating to form an electroless plated film on said exposed wiring pattern and a side wall of said blind via hole;
forming a resist on electroless plated film except for the region of said exposed wiring pattern, a side wall of said blind via hole a step portion of said exposed resin layer;
electro plating to form an electro plated film on said electroless plated film except for said resist; and
removing said resist and subsequently said electroless plated film under said resist.

10. A process as set forth in claim 9, wherein said laser beam irradiating step comprises a step of irradiating a laser beam having a wavelength in the ultraviolet range.

Fig.1(a)

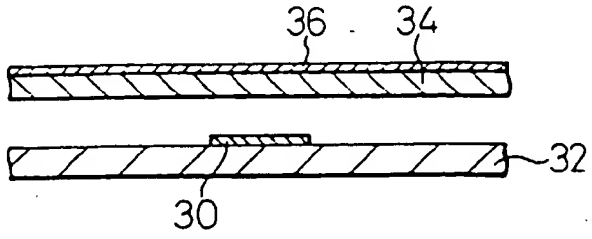


Fig.1(b)

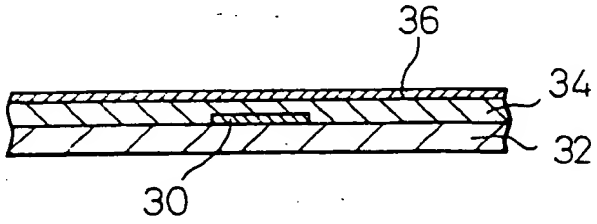


Fig.1(c)

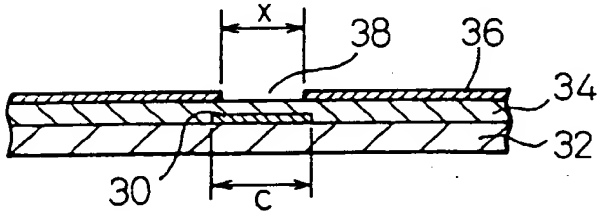


Fig.1(d)

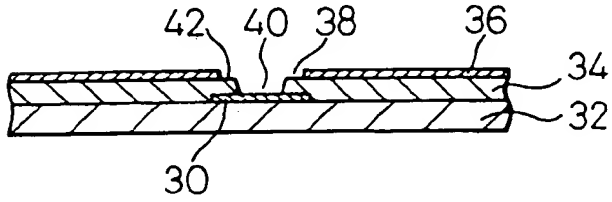


Fig.1(e)

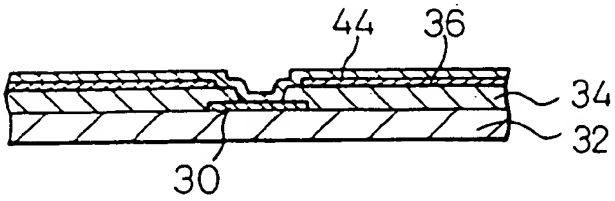


Fig.1(f)

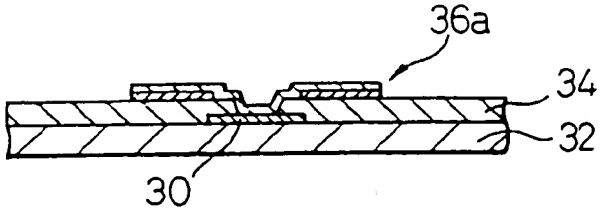


Fig.2(a)

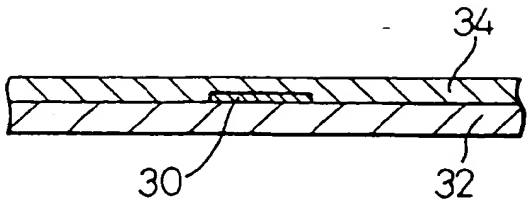


Fig.2(b)

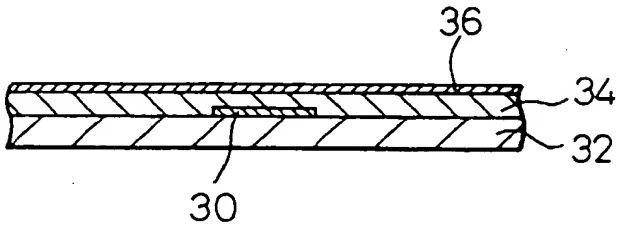


Fig.3

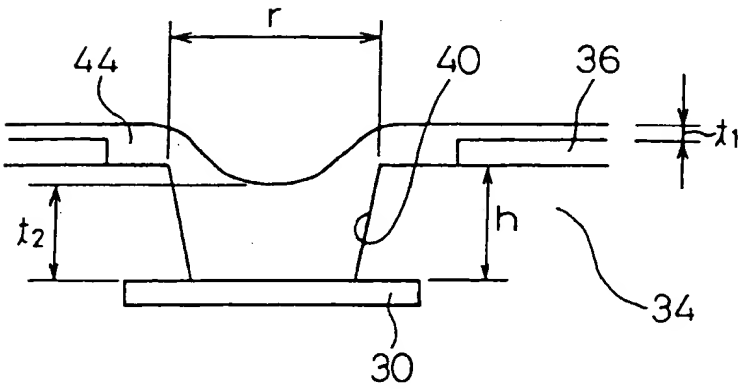


Fig.4(a)

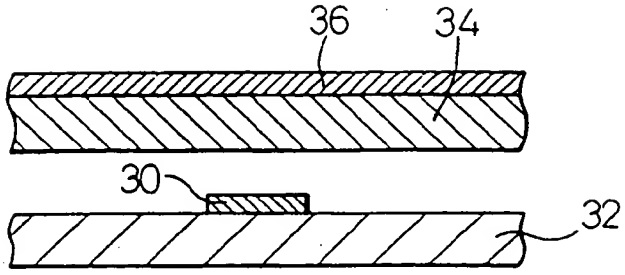


Fig.4(b)

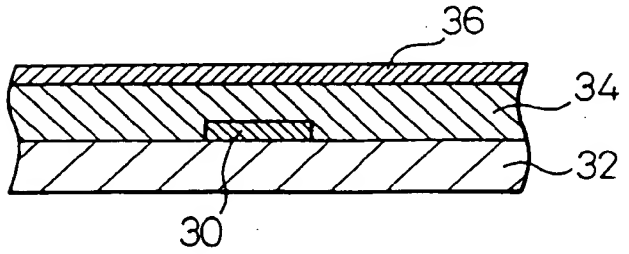


Fig.4(c)

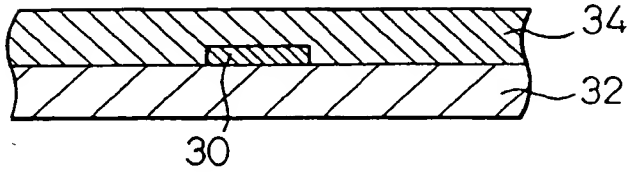


Fig.4(d)

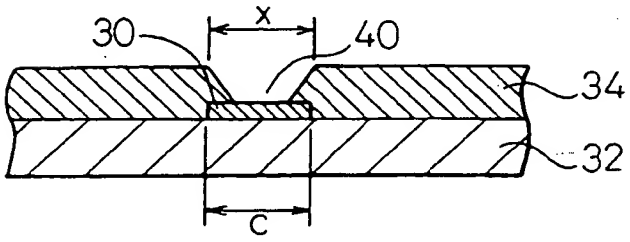


Fig.4(e)

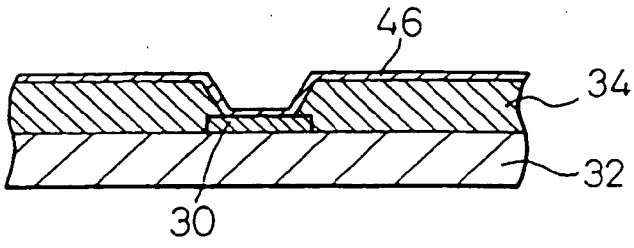


Fig.4(f)

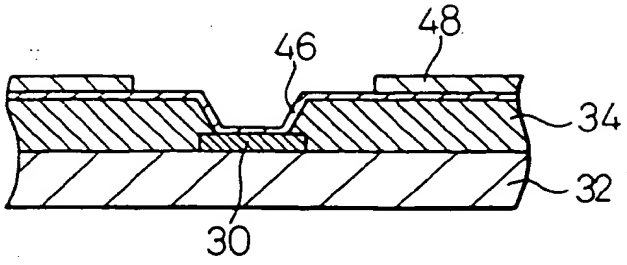


Fig.4(g)

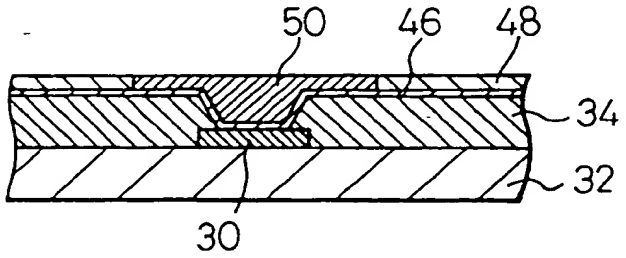


Fig.4(h)

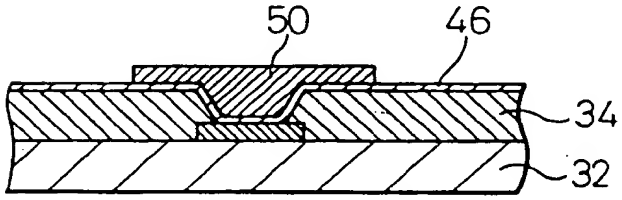


Fig.4(i)

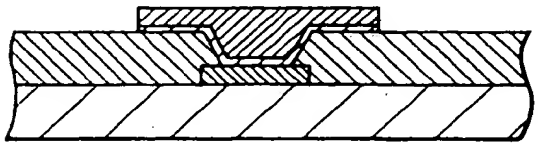


Fig.5(a)
PRIOR ART

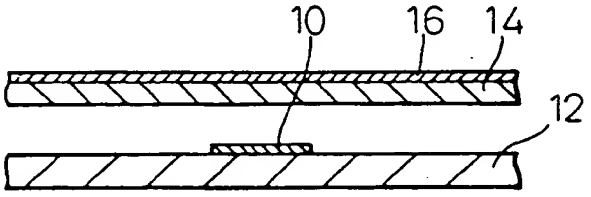


Fig.5(b)
PRIOR ART

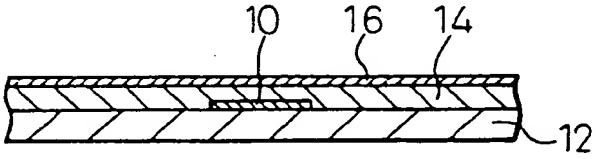


Fig.5(c)
PRIOR ART

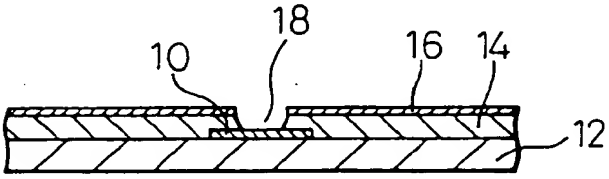


Fig.5(d)
PRIOR ART

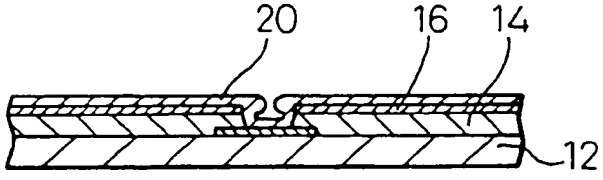


Fig.6(a)
PRIOR ART

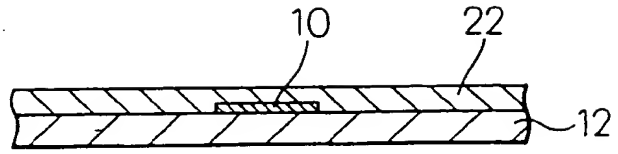


Fig.6(b)
PRIOR ART

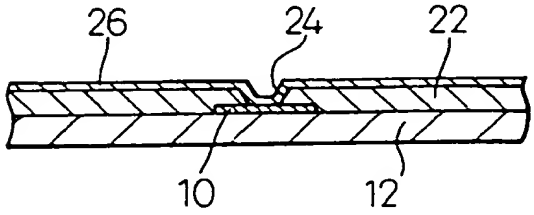
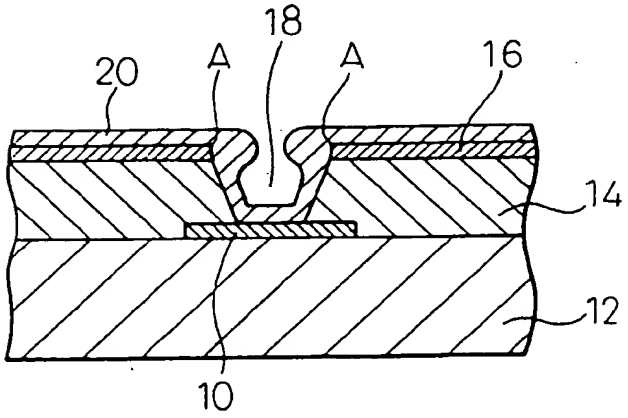


Fig.7
PRIOR ART



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(71) Applicant: SHINKO ELECTRIC INDUSTRIES CO. LTD.
Nagano-shi, Nagano 380-0921 (JP)

(72) Inventors:
- Rokugawa, Akio, c/o Shinko Elec. Ind. Co., Ltd.
Nagano-shi, Nagano 380-0921 (JP)
- Iijima, Takahiro, c/o Shinko Elec. Ind. Co., Ltd.
Nagano-shi, Nagano 380-0921 (JP)
- Nomura, Tomohiro,
c/o Shinko Elec. Ind. Co., Ltd.
Nagano-shi, Nagano 380-0921 (JP)
- Koyama, Toshinori,
c/o Shinko Elec. Ind. Co., Ltd.
Nagano-shi, Nagano 380-0921 (JP)
- Katagiri, Noritaka, Shinko Elec. Ind. Co., Ltd.
Nagano-shi, Nagano 380-0921 (JP)

(74) Representative: Rackham, Stephen Neil
GILL JENNINGS & EVERY,
Broadgate House,
7 Eldon Street
London EC2M 7LH (GB)

(54) Multilayer circuit board

(57) A process for making a multilayer wiring board includes the following steps of: laminating an electrically insulating resin substrate (34), having first and second surfaces and a metal layer (36) formed on the first surface, onto a base material (32) on which a predetermined wiring pattern (30) is formed, so that the second surface of the resin substrate (34) is adhered to the base material (32); removing a predetermined amount (38) of the metal layer (36) to form an opening at a position where a connection with the wiring pattern (30) is to be provided; irradiating a laser beam toward the resin layer (34) through the resin removed region (38) to form a blind via hole (40) having a diameter smaller than that of the opening (38), so that the wiring pattern (30) is exposed at a bottom of the blind via hole (40); electroless plating form an electroless plated film on the exposed wiring pattern (30), a side wall of the blind via hole (40), a step layer (36) at a periphery of the opening (40); electro plating to form an electro plated film on the electroless plated film; and after the electro plating, etching the metal layer to form a predetermined wiring pattern (36a).

Fig.1(d)

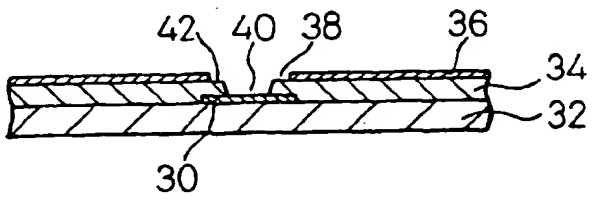

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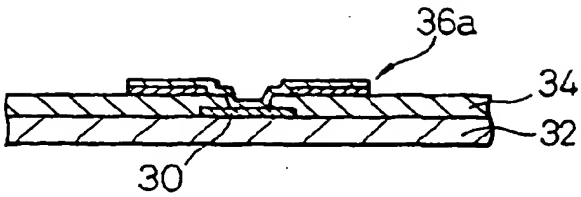
Fig.1(f)



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Application Number
EP 99 30 2743

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28 August 2000	Mes, L

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